ACS APPLIED MATERIALS & INTERFACES

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Improving the Electrical Properties of Lanthanum Silicate Films on Ge Metal Oxide Semiconductor Capacitors by Adopting Interfacial Barrier and Capping Layers

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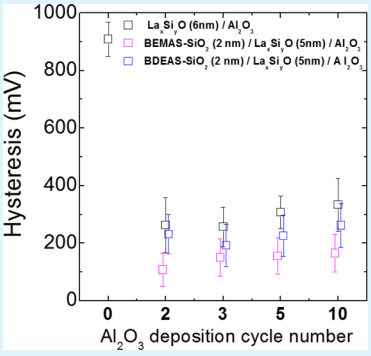
ABSTRACT: The electrical properties of La-silicate films grown by atomic layer deposition (ALD) on Ge substrates with different film configurations, such as various Si concentrations, Al_2O_3interfacial passivation layers, and SiO_2 capping layers, were examined. La-silicate thin films were deposited using alternating injections of the $La[N\{Si(CH_3)_3\}_2]_3$ precursor with O_3 as the La and O precursors, respectively, at a substrate temperature of 310 °C. The Si concentration in the La-silicate films was further controlled by adding ALD cycles of SiO_2. For comparison, La_2O_3 films were also grown using $[La(^iPrCp)_3]$ and O_3 as the La precursor and oxygen source, respectively, at the identical substrate temperature. The capacitance−voltage (C−V) hysteresis decreased with an increasing Si concentration in the La-silicate films, although the films showed a slight increase in the capacitance equivalent oxide thickness. The adoption of Al_2O_3 at the interface as a passivation layer resulted in lower C−V hysteresis and a low leakage current density. The C−V hysteresis voltages of the La-silicate films with Al_2O_3 passivation and SiO_2 capping layers was significantly decreased to ∼0.1 V, whereas the single layer La-silicate film showed a hysteresis voltage as large as ∼1.0 V.



KEYWORDS: *La-silicate, Ge-substrate, Al_2O_3 barrier, SiO_2 capping, hysteresis*

I. INTRODUCTION

Scaling of conventional complementary metal oxide semiconductor (CMOS) transistors using Si as the channel material has driven the integrated circuit industry since the 1970s and is expected to reach its physical limit within the next decade.[1,2] Ge is a feasible candidate for replacing Si as the channel material in p-type metal oxide semiconductor field-effect transistors (MOSFETs) of the post-14-nm technology node because it has a higher hole mobility than Si.[3−6] Similar to SiO_2/Si in Si-MOSFETs, GeO_2/Ge has been generally regarded as the most appropriate interface in Ge-MOSFETs. Nonetheless, the lack of thermodynamic stability at the GeO_2/Ge interface hampers the development of Ge-MOSFETs. Many previous studies have demonstrated that the GeO_2/Ge interface degrades because of desorption of GeO upon thermal annealing above 400 °C under a vacuum or in ambient N_2, owing to an interfacial reaction.[7,8] With atomic force microscopy and thermal desorption spectroscopy studies, the Ge substrate underneath the GeO_2 layer was consumed by the GeO desorption that was produced by a volatilization reaction between GeO_2 and Ge (GeO_2 + Ge → 2GeO).[7−10] Recently, Wang et al. demonstrated an oxygen vacancy diffusion model as the mechanism of GeO volatilization by employing ^{18}O and ^{73}Ge isotope labeling experiments. In those experiments, GeO desorbed from the GeO_2 surface, but the desorption was triggered by an interfacial reaction between Ge and GeO_2. GeO formation was equivalent to the generation of oxygen vacancies (V_o) at the GeO_2/Ge interface in this redox reaction. V_o diffused to the GeO_2 surface, and desorption occurred at the surface of the GeO_2 film.[11] A typical example of electrical degradation by GeO desorption is the large hysteresis in the capacitance−voltage (C−V) curves, which is attributed to electrically active defects near the interface and inside the bulk high-k film.[8] In contrast, thermodynamic calculations have shown that GeO_2 + Ge has a lower Gibbs free energy than 2GeO at a typical processing temperature and pressure (the desorption reaction GeO_2 + Ge → 2GeO has a positive Gibbs free energy change), suggesting that effective isolation of the GeO_2/Ge system from the atmosphere could suppress the reaction at the interface.[12,13] Considering this factor, there could be two possible methods to solve the interfacial reaction problem; one is to adopt a capping layer to isolate the GeO_2/Ge from the atmosphere, and the other is to adopt an interfacial passivation layer (or barrier layer) to physically separate the GeO_2 and Ge. There have been many reports on various interfacial passivation layers, such as ultrathin Si capping layers

Received: February 27, 2014
Accepted: April 15, 2014
Published: April 15, 2014

   dx.doi.org/10.1021/am5012172 | *ACS Appl. Mater. Interfaces* 2014, 6, 7885−7894

on Ge substrates,[14] Ge nitride interfacial layers,[15,16] Al_2O_3 and $LaAlO_3$ dielectric inter layers,[17,18] and high-quality GeO_2 interfacial layers formed by plasma oxidation or high pressure oxidation.[19,20] Among the various passivation techniques, a Si capping layer on a Ge substrate has drawn a great deal of attention because of its superior electrical performance. Cheng et al. reported that a Si capping layer on a Ge substrate retarded the GeO volatilization and suppressed the C−V hysteresis of the HfO_xN_y gate dielectric films in the MOS structure.[21] The decrease in the C−V hysteresis by the Si capping layer was explained by the Si−O bonds having larger Gibbs free energies and higher thermodynamic stabilities than the Ge−O bonds, such that the reaction between the oxide and Ge substrate could be efficiently suppressed.[21] In most of the previous studies, a Si capping layer was formed on a Ge substrate either by epitaxial growth of several monolayers of Si or by annealing in ambient SiH_4 (or Si_2H_4).[21−24] However, not many studies of Si-containing passivation layers grown by an atomic layer deposition (ALD) method on Ge substrates have been reported.

Houssa et al. simulated the atomic configurations of the interface between various rare-earth oxide materials and Ge with first-principles calculations.[25] The results revealed the feasibility of La_2O_3 and Al_2O_3 as an effective passivation layer on Ge to suppress the formation of dangling bonds other than HfO_2. Kato et al. reported that an Al_2O_3 inter layer effectively suppressed the formation of a Ge oxide interlayer in a lanthanum (La) oxide/Al_2O_3/Ge gate stack structure. The formation of GeO_x ($x < 2$) was suppressed by increasing the thickness of the Al_2O_3 interfacial layer up to 1 nm.[26] In contrast, the adoption of a capping layer, which could suppress the volatilization of GeO from the GeO_2 surface, and, thus, the accompanying interfacial reaction, has not been studied in detail compared with the interfacial passivation layer approach. Jung et al. studied various interfacial passivation layers between HfO_2 thin films and Ge substrates to improve the charge trapping properties and the C−V hysteresis characteristics. The SiO_xN_y interfacial passivation layer reduced both the C−V hysteresis and the charge trapping properties. The chemical analysis revealed that the SiO_xN_y passivation interface layer was effective in suppressing the inter mixing between the HfO_2 film and the Ge substrate and the formation of Ge suboxides at the interface.[27]

In this study, ALD of ultrathin Al_2O_3 and SiO_2 layers was adopted as interfacial passivation and capping layers, respectively, with lanthanum-silicate (La-silicate) films on Ge substrates. ALD of the La-silicate films was carried out by sequential injections of the Si containing tris[bis-(trimethylsilyl)amino]lanthanum ($La[N\{Si(CH_3)_3\}_2]_3$) and ozone (O_3) as the La-precursor and the oxygen source, respectively. ALD is the most feasible and competitive process for fabricating high-quality gate dielectric thin films with conformal deposition and high accuracy in the film thicknesses, making it compatible with semiconductor fabrication technologies that are suitable for mass production. During deposition of the La-silicate films, $SiH_2(NC_2H_5CH_3)_2$ (BEMAS) and $SiH_2(N(C_2H_5)_2)_2$(BDEAS) were additionally injected to control the Si concentrations ([Si]/([Si]+[La])) in the high-k films, as well as the accompanying electrical properties. Ultrathin interfacial Al_2O_3 layers whose thicknesses were controlled by deposition cycles (2, 3, 5, and 10 cycles) were formed between the La-silicate film and the Ge substrate by ALD. Additionally, ALD SiO_2 was chosen as the material for the capping layer on the La-silicate films. The multistack of the Al_2O_3 passivation, high-k La-silicate, and capping SiO_2 layers effectively decreased the C−V hysteresis down to 100 mV. This is one of the best results reported to date for a MOS capacitor adopting a Ge substrate. It has to be noted that the primary goal of this work was to elucidate the role of interfacial barrier and capping layers in suppressing the deleterious effects originating from the chemical interactions between the high-k film and Ge substrate. Therefore, relatively thick dielectric films (6−7 nm) were adopted which efficiently suppress other effects that may come from the leakage current and charge trapping.

II. EXPERIMENT PROCEDURE

La-silicate films were grown on a cyclic HF-cleaned Ga-doped p-type (100) Ge substrate at a wafer temperature of 310 °C in a traveling-wave-type 4-inch-diameter scale thermal ALD reactor with a liquid delivery system using $La[N\{Si(CH_3)_3\}_2]_3$ dissolved in hexane (0.15 mol/L) as the La precursor. Various passivation interfacial layers and capping layers, such as Al_2O_3, SiO_2, and La_2O_3, were also deposited by ALD. $Al(CH_3)_3$(TMA), BEMAS, BDEAS, and (tris(isopropyl-cyclopentadienyl)lanthanum) ($La(^iPrCp)_3$) were used as the metal precursors for Al_2O_3, SiO_2, and La_2O_3, respectively. O_3 with a concentration of 110 g/Nm^3 was used as the oxygen source for the La-silicate, Al_2O_3, SiO_2, and La_2O_3 films. $La[N\{Si(CH_3)_3\}_2]_3$was vaporized at 190 °C and delivered to the reactor with help from an Ar carrier gas of 200 standard cubic centimeter per minute (sccm). The injection time for the $La[N\{Si(CH_3)_3\}_2]_3$ precursor solution was controlled in milliseconds to precisely deliver it to the vaporizer. The precursor injection time for the La-silicate, La_2O_3, SiO_2, and Al_2O_3 sources and the O_3 were fixed at 0.1 ms and 10, 1, 1, and 5 s, respectively. Under these conditions, the growth rates of the La-silicate, La_2O_3, SiO_2, and Al_2O_3 films were 0.08, 0.085, 0.09, and 0.1 nm/cycle, respectively. Under these conditions, the growth of the 1-nm-thick La-silicate and SiO_2 films required 416 and 188 s, respectively. To control the Si concentration in the La-silicate films, a Si precursor was injected alternately during the La silicate film deposition. The thickness of the Al_2O_3 passivation layer was controlled by the deposition cycles, from two cycles to 10 cycles (∼1 nm), and the SiO_2 capping layer was fixed at 2 nm. The base pressure of the ALD chamber was maintained below 0.01 Torr, and the operational pressure was ∼0.3 Torr. The film thicknesses were measured with an ellipsometer (ESM-300; J.A. Woollam Co., Inc.) and X-ray reflectivity (PANalytical; X'Pert PRO MPD) and were confirmed by high-resolution transmission electron microscopy (HRTEM; JEOL, JRM 2100F). The depth profiles of the elements in the films were examined by Auger electron spectroscopy (AES; PerkinElmer 660). The chemical states and electronic structures of the films were analyzed by X-ray photoelectron spectroscopy (XPS; Sigma Probe) using monochromatic Al Kα as the X-ray source. All of the examined samples did not undergo post-deposition annealing after the film growth, and forming gas annealing was not carried out after deposition of the top electrode. This was performed so that no intermixing between the deposited layers was induced, allowing for clear identification of the role of the different layers and the film compositions on the chemical structure and accompanying electrical properties. Therefore, it is anticipated that appropriate annealing of the films before and after deposition of the electrode could further improve the electrical performance, although the optimized sample structures reported in this work already exhibited an impressive electrical performance without any thermal treatment. This examination is on-going and will be reported elsewhere.

For MOS capacitor fabrication, Pt top electrodes were deposited by electron-beam evaporation using a shadow mask. C−V curves, constant-voltage stress (CVS), and the interface state density (D_{it}) were evaluated with a conductance method, and the leakage current density-voltage (J_g-V) characteristics were measured using a HP 4284 LCR meter and a HP 4140B picoammeter/DC voltage source, respectively. The capacitance equivalent thickness (CET) was

calculated from the accumulation capacitances measured at 1 MHz, taking quantum mechanical effects into consideration. A voltage was applied to the Pt top electrode, while the Ge substrate was grounded via an In contact.

III. RESULTS

III-1. Effects of the Si-Concentration in La-Based Oxide Films. The structure and electrical properties of single layer La-silicate films were examined for different Si concentrations. In this set of experiments, the La_2O_3 films were deposited using $La(^iPrCp)_3$ as the precursor. The La-silicate films were deposited using $La[N\{Si(CH_3)_3\}_2]_3$, and the Si-concentration controlled La-silicate films were deposited by alternative injections of $La[N\{Si(CH_3)_3\}_2]_3$ and either BEMAS or BDEAS precursors. The Si concentrations in the as-deposited La-silicate films using only $La[N\{Si(CH_3)_3\}_2]_3$ as the precursor were ~25%, which was confirmed with an Auger depth profile, as shown in Figure 1b. The Si concentrations

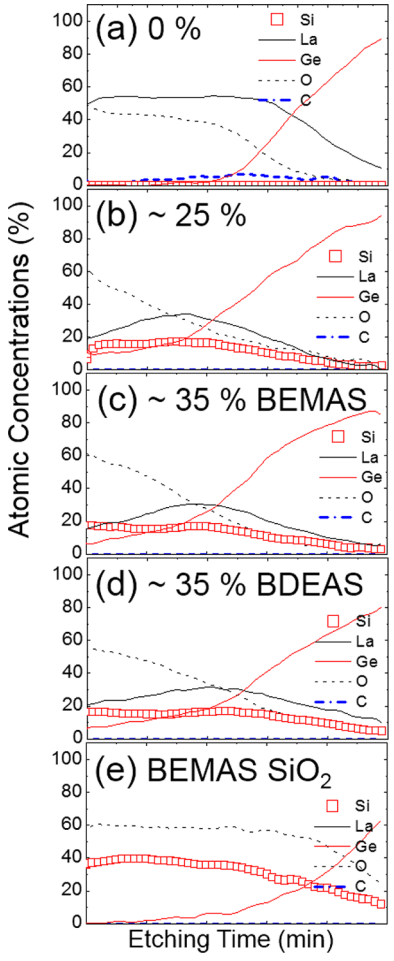


Figure 1. AES depth profiles of (a) La-oxide thin film, (b) La-silicate thin film, Si concentrations controlled La-silicate film by (c) BEMAS-Si precursor, (d) BDEAS-Si precursor, and (e) SiO_2 thin film by BEMAS precursor.

were obtained using the average concentrations of La and Si through the oxide layer in the AES results. Figure 1a showed that the Si concentrations for the pure La_2O_3 thin films deposited using $La(^iPrCp)_3$ as the precursor were below the detection limit of the AES (< ~1%). The concentration of Ge in the La_2O_3 films was also minimized under this condition. The ALD cycle ratio of the SiO_2 and La silicate was controlled to make the Si concentration in the La-silicate films ~35% (Figure 1c and d, where BEMAS and BDEAS were adopted, respectively). The Ge-concentration in the La-silicate film was significantly observed up to the film surface. Figure 1e shows the AES depth profile of an ALD SiO_2 film using BEMAS as the precursor, which revealed that the Ge concentration was not negligible, especially near the interface, but it was negligible near the film surface. From the AES results in Figure 1, the Ge concentration in the La-silicate film was much higher than in the non-doped La_2O_3 and SiO_2 films, while the Ge concentration was almost independent of the Si concentration under the experimental conditions used. To understand the influence of the chemical changes in the films, C–V measurements were performed for a given oxide film (physical) thickness of ~6 nm, which included the thickness of the interfacial layer. The C–V hysteresis and CET values were examined from the C–V curves when the gate voltage was swept from the depletion region (positive voltage) to the accumulation region (negative voltage) and back to the depletion region. The C–V hysteresis was extracted from the flat band voltage difference in the two C–V curves during the forward and reverse sweeps. Figure 2 shows the variations in

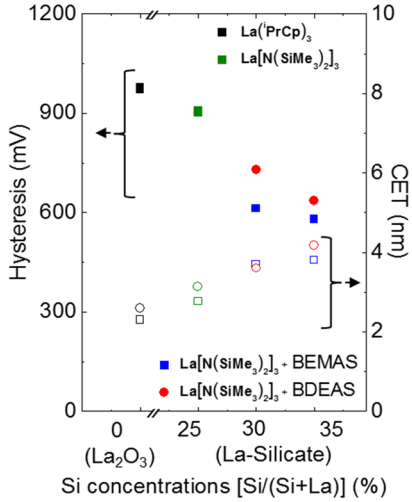


Figure 2. C–V hysteresis and CET as a function of Si concentrations of La-based oxide films.

the C–V hysteresis voltage (left hand ordinate, closed symbols) and the CET (right hand ordinate, open symbols) of the oxide films as a function of the Si concentration. The CET increased slightly with an increasing Si concentration in the La-silicate films because of the decreased k value of the oxide layer, while the hysteresis voltage decreased rapidly with an increasing Si concentration. These tendencies were not dependent on the type of Si precursor used for the La-silicate film growth. When the high-k films were deposited directly onto the HF cleaned Ge substrates, a significantly large C–V hysteresis of ~1000 mV was observed, suggesting that a high density of electrically active defects was created near the interface or inside the bulk high-k film, which is consistent with a previous report.[18] This suggests that the non-doped film underwent a severe interfacial reaction, resulting in a higher trap density either near the interface or inside the bulk film. Incorporation of Ge into the high-k film could be induced in two ways; one was the solid-state diffusion of Ge atoms (or ions) from the Ge substrate to

dx.doi.org/10.1021/am5012172 | ACS Appl. Mater. Interfaces 2014, 6, 7885–7894

the film, and the other was the trapping of GeO, which was produced by the desorption reaction ($GeO_2 + Ge \rightarrow 2GeO$) at the interface with the Ge-substrate and volatilization of the GeO. Some of the volatilized GeO was trapped in the film during ALD of the high-*k* films. More details on this aspect of Ge-incorporation are presented in the Discussion section. Among the two mechanisms, the latter is believed to be largely responsible for the Ge-incorporation in the high-*k* films because there is no obvious reason for how the La_2O_3 film could sufficiently suppress the solid-state diffusion of Ge. The almost negligible Ge concentration in the La_2O_3 film therefore suggests that the La_2O_3 layer cannot prevent volatilization of the GeO that was produced by the desorption reaction at the interface, which could cause the high interfacial defect density. In contrast, when the Si concentration of the La-silicate film was increased from 0% to ~35%, the C−V hysteresis was decreased by ~40% and the hysteresis voltage became ~600 mV when the Si concentration was ~35%. The relatively high Ge concentration in the film suggested that the volatilization of GeO from the film surface was suppressed, inducing fewer interfacial reactions with the Ge substrate.

To achieve a better understanding of this behavior, the chemical bonding states of various La-silicate films on Ge substrates were examined by XPS. The degree of formation of the Ge oxides was focused on with XPS. Figure 3a shows the

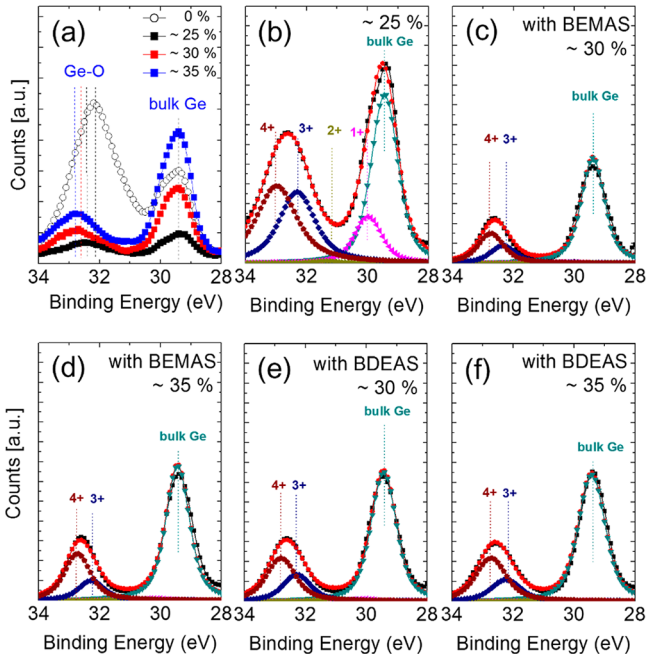


Figure 3. Ge 3d core level of (a) various Si concentration of La-based oxide film using BEMAS precursor, the explicit deconvolution for Ge-oxide for (b) pure La-silicate film and (c) ~30 % and (d) ~35 % Si concentrations controlled La-silicate films using BEMAS precursor, and (e) ~30 % and (f) ~35 % Si concentrations controlled La-silicate films using BDEAS precursor.

Ge 3d spectra of pure-La_2O_3 and La-silicate films with Si concentrations of ~25%, 30%, and 35%, where BEMAS was adopted as the Si precursor. The energy scale was calibrated by fixing the Ge 3d peak of the bulk Ge (Ge^0) at a binding energy (BE) of 29.4 eV, which was clearly observed because the thickness of the high-*k* films was thin enough such that it did not greatly attenuate the photoelectrons generated from the Ge-substrates. This also suggested that the BE-shifted Ge 3d signal originated not only from the oxide layer but also from the interfacial layer. A clear peak at a BE higher than that of bulk Ge was observed, and the BE shifts of the Ge-oxide peak from the Ge^0 were 2.91, 3.12, 3.27, and 3.43 eV for La_2O_3 for La silicates with Si concentrations of 25%, 30%, and 35%.

The lack of a Ge signal in the La_2O_3 layer in Figure 1a revealed that the oxidized Ge 3d peak in the XPS mainly originated from the Ge-oxide layer located at the interface between the La_2O_3 film and Ge substrate. To understand the variations in the chemical states of the films with different Si concentrations, the Ge 3d peaks were deconvoluted, assuming the presence of five Ge oxidation states (Ge^0, Ge^{1+}, Ge^{2+}, Ge^{3+}, and Ge^{4+}), the spectra related to the Ge oxide could be deconvoluted into four Ge oxide peaks (Ge^{1+}, Ge^{2+}, Ge^{3+}, and Ge^{4+} with BE shifts from the bulk Ge 3d of 0.8, 1.8, 2.6, and 3.4 eV, respectively[28,29]). These results are included in Figure 3b−f. After subtracting the background intensities, the area of each peak was calculated, and the (Ge^{4+} peak)/(sum of Ge^{1+}, Ge^{2+}, and Ge^{3+} peaks) ratios were found. Figure 3b−f show the variations in the ratio as a function of the Si concentration in the La_2O_3 and La-silicate films. Figure 3 also includes the corresponding results achieved with the La-silicate films that adopted BDEAS. The ratios were almost independent of the type of Si precursor used, but they were largely determined by the Si concentration and increased with an increasing Si concentration. The generation of Ge suboxides is considered to contribute to the large hysteresis voltage in the C−V curves as well as the fast interface trap states (D_{it}), even at the cost of increasing the CET.[10] These results suggest that higher Si concentrations in the La-silicate films suppressed the Ge suboxide formation at the Ge interface, which was effective in decreasing the C−V hysteresis voltage.

Figure 4 shows variations in the C−V curves with different stress times for CVS tests (with a gate stress voltage of −2.5 V)

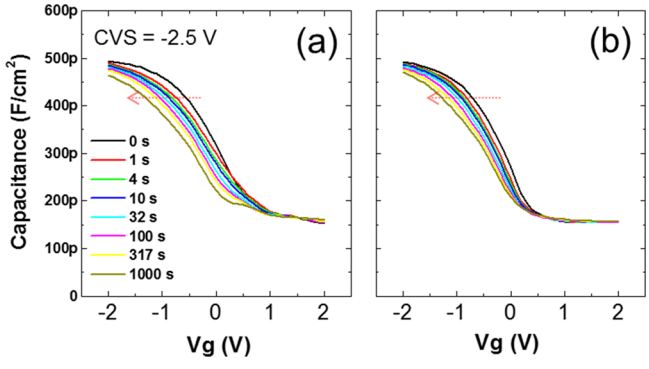


Figure 4. C−V curves for CVS (with a gate stress voltage of −2.5 V) on MOSCAPs with the structures of (a) Pt/La-oxide/*p*-Ge and (b) Pt/La-silicate (~25 % Si concentration)/*p*-Ge.

on MOS capacitors with structures of (a) Pt/La_2O_3/p-Ge and (b) Pt/La-silicate (Si concentration of ~25%)/p-Ge. The C−V curves were recorded for fresh samples under forward and reverse bias sweeps with a gate voltage sweep rate of 50 mVs^{-1} and after eight successive stress cycles (0, 1, 4, 10, 32, 100, 317, and 1000 s). The flat-band voltage shift (ΔV_{FB}), which is related to the fixed charge trapping in the devices, and the slope change of the C−V curve, which is related to the generation of D_{it}, were determined from the figure. The La-oxide film had a large ΔV_{FB} in the negative voltage direction as well as changes

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in the slopes of the C−V curves, while the La-silicate film had a notable change in the slopes of the C−V curves. This suggests that the deterioration of the bulk properties in the La_2O_3 films (fixed charge generation) was higher than in the La-silicate films, while the degradation of the interfacial trap properties was similar. The La-oxide film had a larger C−V hysteresis than the La-silicate film. This was mainly caused by a larger number of trapped charges in the bulk, and the contribution of the interface trap density could be similar to that of La silicate. The XPS and CVS results suggested that the higher Si concentration in the La-silicate films suppressed the formation of Ge suboxides at the Ge interface and bulk traps in the films, which was effective in decreasing the C−V hysteresis.

III-2. Adoption of an Al_2O_3 Interface Passivation Layer. To further improve the quality of the interface, and thus decrease the C−V hysteresis, a thin Al_2O_3 layer was inserted between the La-silicate film (25% Si concentration) and the Ge substrate. In this experiment, no additional Si-precursor injection was performed during the high-*k* film growth. The thickness of the Al_2O_3 layer was varied by changing the deposition cycles from 2 to 10 cycles, with 10 deposition cycles being coincident with a ∼1-nm-thick Al_2O_3 film. MOS capacitors (MOSCAPs) with ∼6-nm-thick La-silicate films with a thin Al_2O_3 passivation layer were fabricated. The C−V curve shifted toward the positive voltage direction with an increasing number of Al_2O_3 deposition cycles, because there were negative fixed charges in the Al_2O_3 films.[30,31] Figure 5 shows the variations in the C−V hysteresis voltages for the

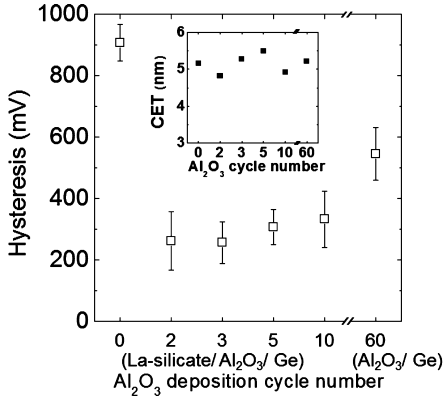

Figure 5. C−V hysteresis of La-silicate MOSCAPs with an ultrathin Al_2O_3 passivation interface layer as a function of Al_2O_3 deposition cycles. Inset figure shows CET changes as a function of Al_2O_3 deposition cycles.

La-silicate films as a function of the number of Al_2O_3 deposition cycles and Al_2O_3 films (60 cycles ∼6 nm). The data without an Al_2O_3 cycle were taken from Figure 2. When there were two and three Al_2O_3 deposition cycles, a passivation interface layer was inserted between the La-silicate and the Ge substrate, and the C−V hysteresis had its lowest value (∼250 mV). Further increasing the number of Al_2O_3 cycles increased the value to ∼350 mV when 10 cycles were adopted. The C−V hysteresis of a ∼6-nm-thick Al_2O_3 layer was ∼550 mV, suggesting that the appropriate combination of the La-silicate layer and the interfacial passivation Al_2O_3 layer (2−3 cycles) was required to decrease the C−V hysteresis. Inset figure shows the CET values of the various samples in Figure 5. There were variations in the CET values for the different samples, but the degree of variation (∼0.5 nm) was not large.

Figure 6a−c show the AES depth profiles, 6.0 nm in thickness, for Al_2O_3, La-silicate with Al_2O_3 (with two cycles),

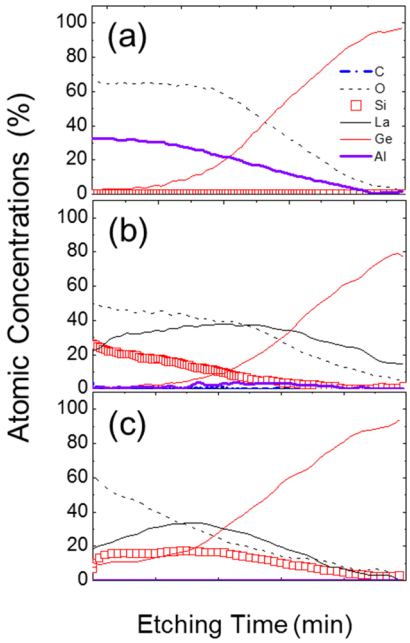

Figure 6. AES depth profiles of (a) Al_2O_3/*p*-Ge, (b) La-silicate/Al_2O_3 (2 cycles)/*p*-Ge, and (c) La-silicate/*p*-Ge.

and La-silicate films, respectively. The Al_2O_3 film had almost no impurities in the bulk film, proving its effective barrier properties against GeO volatilization and Ge diffusion, but there could also be an interfacial reaction. This can be understood from the tailed Ge distribution near the interface. The adoption of Al_2O_3 cycles, even though the Al_2O_3 layer was ultrathin, decreased the Ge concentration within the La-silicate film, and the density of defect centers related to Ge in the La-silicate film was decreased.

The chemical states in the films were further examined with XPS. The Ge 3d peaks and the deconvoluted results for La-silicate films with the different Al_2O_3 cycles are shown in Figure 7. The films generally showed oxidized Ge 3d peaks. The ratios of (Ge^{4+} peak)/(sum of Ge^{1+}, Ge^{2+}, and Ge^{3+} peaks) were calculated using the same method as in Figure 3b−d for different Si concentrations in the La-silicate films. The values for 2, 3, 5, and 10 Al_2O_3 cycles were 46%, 42%, 39%, and 35%, respectively. In Figure 3b, the ratio for the La-silicate film with a Si concentration of 25% was ∼40%. It increased to 46% in Figure 7 when only two Al_2O_3 cycles were adopted before the La-silicate film was deposited. Therefore, the improvement in the C−V hysteresis (shown in Figure 5) can be understood because less Ge was incorporated into the bulk of the La-silicate films and there was lesser of defective Ge-oxide at the interface. However, a further increase in the number of Al_2O_3 cycles decreased the ratio, suggesting that there was an increase in the formation of Ge suboxides, which is consistent with the degraded C−V hysteresis performance shown in Figure 5.

Hinkle et al. and Milojevic et al. reported that the thickness of the native oxide formed on GaAs and Ge substrates decreased after Al_2O_3 was deposited by the ALD method using TMA and H_2O.[32,33] These reports suggested that the decrease in the thickness of the oxide inter layers was caused by the strong reduction of the TMA precursor.[32,33] It is believed that

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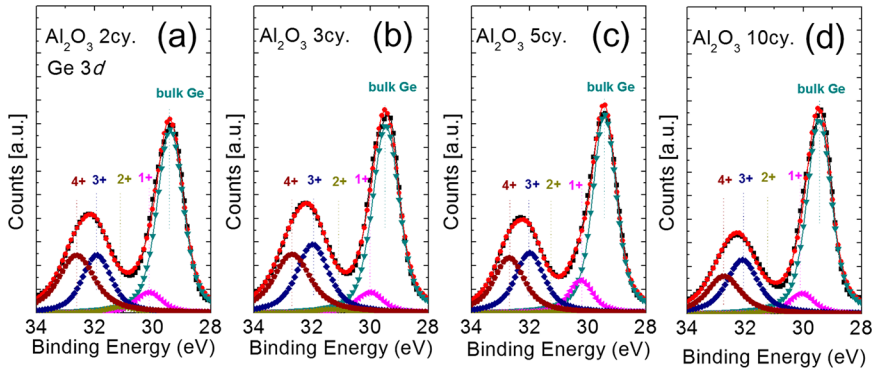

Figure 7. Ge 3d core level for the explicit deconvolution for Ge-oxide (a) La-Silicate/Al_2O_3 (two cycles)/*p*-Ge, (b) La-silicate/Al_2O_3 (three cycles)/*p*-Ge, (c) La-silicate/Al_2O_3 (five cycles)/*p*-Ge, and (d) La-silicate/Al_2O_3 (10 cycles)/*p*-Ge.

the same interfacial cleaning effect occurred for the optimum number of Al_2O_3 cycles (two to three cycles), while further increasing the number of Al_2O_3 cycles (more than five cycles) deteriorated the interfacial properties with the formation of the sub-oxides.

To further study the interfacial properties of the La-silicate films, the Al_2O_3 passivation (two cycles) interface with La-silicate, and Al_2O_3 films, the D_{it} was extracted using a conductance method. Figure 8a shows the D_{it} of the three

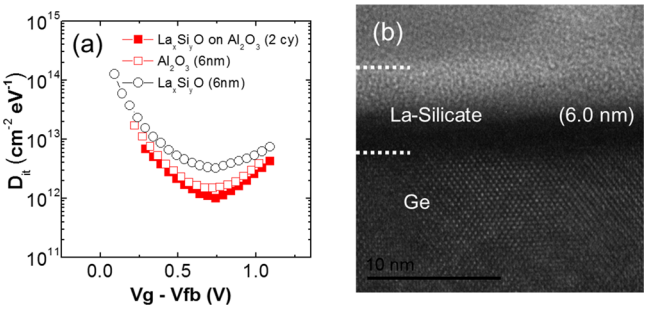

Figure 8. (a) Interface state density vs. V_g–V_{FB} of Al_2O_3/Ge, La-silicate/Al_2O_3 (two cycles)/Ge, and La-silicate/Ge and (b) TEM images for La-silicate/Ge.

samples as a function of the gate voltage-flat band voltage (V_g–V_{FB}). Al_2O_3 passivation of the La-silicate films had the smallest D_{it} among the films studied, suggesting that the ultrathin Al_2O_3 passivation film effectively reduced the interfacial state density. Figure 8b shows a cross-sectional TEM image of the La-silicate film, confirming the thickness was ~6 nm and the film maintained an amorphous structure. The two films also had a similar thickness and structure (TEM images not shown).

CVS tests with a V_g of −2.5 V were performed on the three samples. Figure 9 shows the results for (a) Pt/La-silicate/p-Ge, (b) Pt/La-silicate with an Al_2O_3 passivation layer (two deposition cycles)/p-Ge, and (c) Pt/Al_2O_3/p-Ge. While the single-layer La-silicate and the Al_2O_3 film showed D_{it} degradation (decreasing slope in the C−V curves) and positive charge trapping (parallel shift in the C−V curve in the negative direction), the La-silicate film with an Al_2O_3 passivation layer with two cycles showed improved reliability characteristics; it did not show any notable changes in the V_{FB}, whereas degradation in the D_{it} was still persistent. This result indicated that the Al_2O_3 film had a large bulk trap density, which induced the large C−V hysteresis, irrespective of the interfacial properties with the Ge substrate. The C−V hysteresis was governed by both the interfacial properties with the Ge substrate and the oxide bulk trap density. These variations in the chemical composition and structure at the interface and in the bulk film, and the accompanying electrical performance, must be closely related to the formation of GeO and its volatilization from the interface or the bulk film. Once volatilization occurred, identifying the GeO formation became difficult via chemical analyses such as AES and XPS. Therefore, capping of the La-silicate film with a thin SiO_2 layer was performed. The SiO_2 capping layer also largely improved the electrical properties.

III-3. Multistacked La-Silicate Films with an Al_2O_3 Passivation Layer and a SiO_2 Capping Layer. A SiO_2 layer with a thickness of 2 nm was deposited on the 5 nm-thick La-silicate films (25% Si concentration) with different Al_2O_3 passivation layer cycles (2−10 cycles) using BEMAS or BDEAS

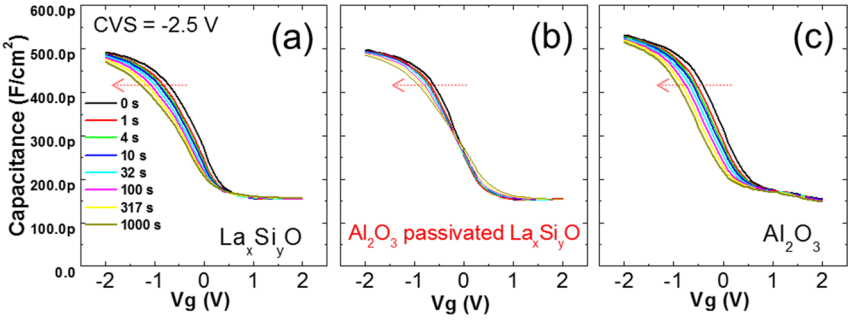

Figure 9. C−V curves of CVS on MOSCAPs with the structures of (a) Pt/La-silicate/Ge, (b) Pt/La-silicate/Al_2O_3 (two cycles)/Ge, and (c) Pt/Al_2O_3/Ge.

Si precursors to examine the effects of capping the high-k film with a thin SiO_2 layer. Figure 10 shows the variations in the C–V hysteresis for the three sets of samples as a function of the number of Al_2O_3 ALD cycles: La-silicate with only an Al_2O_3 passivation layer and two different types of SiO_2 capping layer with Al_2O_3 passivated La-silicates. The data for La-silicate with only an Al_2O_3 passivation layer were reproduced from Figure 5 for a comparison. The SiO_2 capping layer was generally an effective method in decreasing the C–V hysteresis voltage. Adoption of the BEMAS Si-precursor was especially effective in decreasing the C–V hysteresis, and a minimum value of ~100 mV was observed with the optimum number of Al_2O_3 cycles of two. Among the many samples tested under this condition to obtain statistically meaningful data, one sample showed a hysteresis voltage as small as 50 mV. Therefore, SiO_2 capping in combination with Al_2O_3 passivation with the optimum number of cycles is a promising method in decreasing the C–V hysteresis in the high-k gate stack films on Ge substrates.

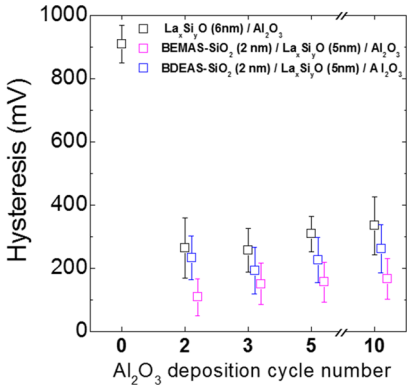

Figure 10. C–V hysteresis of La-silicate MOSCAPs with BEMAS and BDEAS SiO_2 capped La-silicate with Al_2O_3 interface passivation layer on Ge as a function of Al_2O_3 deposition cycles.

Figure 11 shows AES depth profiles for (a) BEMAS and (b) BDEAS SiO_2-capped La-silicate layers with an Al_2O_3 (two cycles) interface passivation layer on Ge. The compositions of the deposited films were almost identical for both SiO_2 capping layers. The presence of the thin SiO_2 capping layer caused the Si concentration in the La-silicate to appear to be higher than that with no SiO_2 capping layer, which is believed to be a result of the limited depth resolution of the AES system. A comparison between the AES depth profiles with the data for the samples with no SiO_2 capping layer (Figure 6b and c) showed that the Ge concentration in the SiO_2-capped La-silicate film was higher, which is almost comparable to the La-silicate films with no capping layer and an Al_2O_3 passivation layer shown in Figure 1b–d. This was unexpected since the adoption of an Al_2O_3 passivation layer suppressed the Ge-concentration in the La-silicate films (Figure 6), and the SiO_2 layer did not induce high Ge concentrations in the SiO_2 films either (Figure 1e). Considering the processing conditions for the sequential deposition of ultrathin Al_2O_3/5-nm-thick La-silicate/2-nm-thick SiO_2, the Ge concentration in the high-k film must have been low when the ultrathin Al_2O_3/5-nm-thick La-silicate films were deposited. Therefore, the higher Ge concentration must have been induced during the final SiO_2 deposition step. This aspect is discussed in detail in the Discussion section.

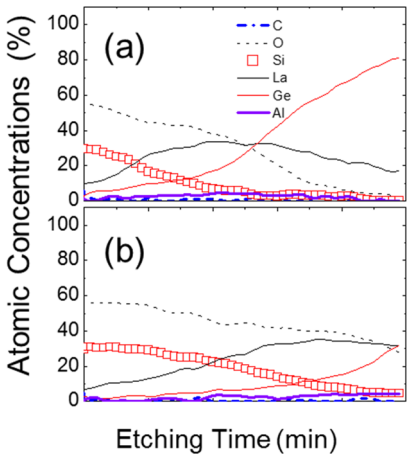

Figure 11. AES depth profiles for (a) BEMAS and (b) BDEAS SiO_2 capped La-silicate with Al_2O_3 (two cycles) interface passivation layer on Ge.

Figure 12a shows the D_{it}'s for BEMAS and BDEAS SiO_2-capped La-silicate layers with an Al_2O_3 interface passivation layer as a function of the V_g–V_{FB}. BEMAS-SiO_2-capped La-silicate with an Al_2O_3 interface passivation layer had a lower D_{it} than the BDEAS-SiO_2-capped sample. A minimum D_{it} of less than 10^{12} cm^{-2} eV^{-1} was achieved for the best condition. Figure 12b and c show cross-sectional HRTEM images for the BEMAS- and BDEAS-SiO_2-capped La-silicate with an Al_2O_3 (two cycles) interface passivation layer on Ge. Although the detailed film structure was difficult to see because of the inappropriate TEM sample quality, the total thickness of ~7 nm, which was expected from the thickness of the La-silicate (5 nm) and SiO_2 (2 nm) films, could be estimated for both cases.

The C–V curves for the CVS tests on Pt/BEMAS SiO_2 2 nm/La-silicate 5 nm/Al_2O_3 (two cycles)/p-Ge and Pt/BDEAS SiO_2 2 nm/La-silicate 5 nm/Al_2O_3 (two cycles)/p-Ge are shown in Figure 13a and b, respectively. The BEMAS-SiO_2-capped multistack layer had small changes in the slopes of the C–V curves, suggesting that degradation of the D_{it} was minimized in this sample, while that in the BDEAS-SiO_2-capped sample had a slightly more severe change in the slope. The C–V hysteresis after CVS tests for 1000 s for the BEMAS-SiO_2-capped sample remained identical to the V_{FB} shift of the initial position, suggesting that the sample was robust against electrical stress.

Figure 14 shows a summary of the leakage current (J_g, measured at V_{FB} − 1 V) vs the CET for the samples discussed in this work. Because of the generally high physical thickness and the accompanying CET, this did not have significant importance in estimating the dielectric performance of the samples. However, it can be confirmed that the multistack sample with a BEMAS SiO_2 capping layer showed a stable leakage current at a CET of 5 nm, which is not necessarily the case for the Al_2O_3 or BDEAS-SiO_2-capped samples.

VI. DISCUSSIONS

The Ge impurities in the high-k dielectric films with various oxidized forms acted as the defect centers, which deteriorated the electrical performance. However, as mentioned in the previous section, the incorporation of Ge into the high-k film appeared to originate not from the solid-state diffusion from the Ge substrate but from the trapping of volatile GeO during the ALD process. This is different from the Si substrate where Si diffusion almost always occurred during high-k film growth or

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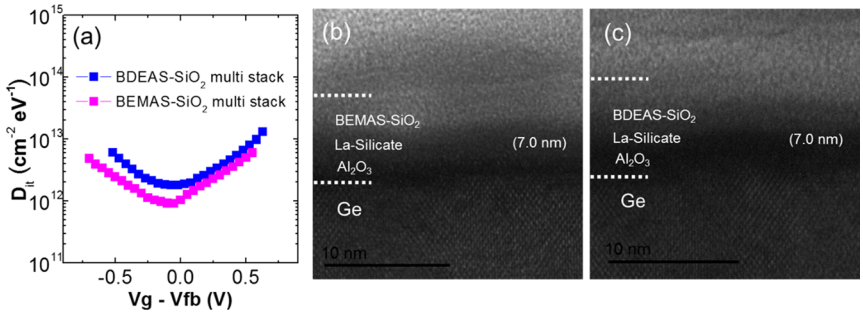

Figure 12. Interface state density vs. $V_g - V_{FB}$ for (a) BEMAS and BDEAS SiO_2 capped La-silicate with Al_2O_3 (two cycles) interface passivation layer on Ge. TEM images for (b) BEMAS and (c) BDEAS SiO_2 capped La-silicate Al_2O_3 (two cycles) interface passivation layer on Ge.

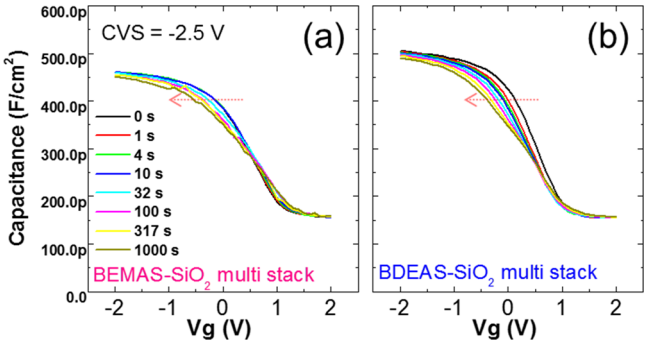

Figure 13. C–V curves for CVS on (a) BEMAS and (b) BDEAS SiO_2 capped La-silicate with Al_2O_3 (two cycles) interface passivation layer on Ge.

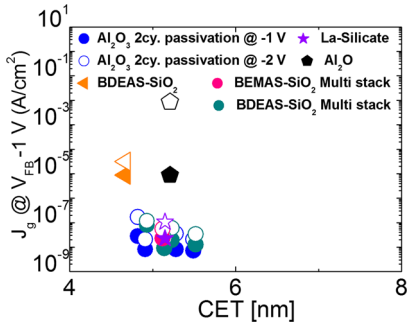

Figure 14. Insulating properties for various high-k thin films deposited with thermal ALD.

post-deposition annealing.[34] The significant Si diffusion was mainly ascribed to the higher oxide formation energy of SiO_2 compared with that of GeO_2. Thus, the driving force for the Si diffusion was not just the concentration gradient of Si but the tendency to form SiO_2. It has been observed that an ultrathin SiO_2 layer was formed, even on high-k HfO_2 film surfaces, after post-deposition annealing by the diffusion of Si from the Si substrate to the film surface, where it oxidized.[34] This was also the main reason why an interfacial reaction for the formation of volatile SiO ($SiO_2 + Si \rightarrow 2SiO$) was highly unlikely.

The key to suppressing the incorporation of Ge atoms (or ions) into the high-k film was to suppress the desorption reaction between GeO_2 and Ge. During ALD of high-k oxides, the highly reactive O_3 was adopted as the oxygen source, and the thermodynamic and kinetic environments for this reaction were quite complicated. It is believed that the desorption reaction is in competition with the GeO_2 formation reaction by the strong oxidation power of O_3. In addition, there must always be a native oxide, which is vulnerable to inducing the desorption reaction. Therefore, to correctly interpret the experimental results in section III, understanding these complicated reactions is necessary. Unfortunately, this is generally not easy because once GeO becomes volatile, it cannot be traced by any chemical analysis tools, such as AES or XPS. The pure La_2O_3 film shown in section III-1 serves as a representative example for this difficulty; the film did not contain any notable Ge impurities, but the electrical performance was the lowest among the samples tested. This must have been caused by the low blocking performance of the pure La_2O_3 film to the volatilization of GeO that was produced at the high-k/Ge interface during ALD of the La_2O_3 film. As the GeO can be easily removed from the interface through the La_2O_3 film, the desorption reaction ($GeO_2 + Ge \rightarrow 2GeO$) kept occurring and the interface and the high-k film bulk deteriorated. In contrast, the La-silicate films had more efficient properties of blocking the GeO diffusion through them, so they could contain a substantial amount of Ge (or GeO_x). Under this circumstance, the partial pressure of GeO at the interface must be higher than that for the La_2O_3 film, so that the progression rate of the desorption reaction can be retarded, inducing an improved electrical performance. By the extension of this consideration on the desorption reaction, the results from the Al_2O_3 passivation and SiO_2 capping can be understood.

When the Al_2O_3 passivation layer is considered, however, another complication becomes involved as the high reactivity of TMA can remove the native GeO_2 by reduction. The almost negligible Ge concentration in the La-silicate film when two to three Al_2O_3 passivation ALD cycles were adopted suggests that the native GeO_2 was effectively removed and that the desorption reaction that originated from the native GeO_2 layer could be largely suppressed. This in turn suggests that the incorporated Ge in the La-silicate films (shown in Figure 1b–d) mainly originated from the desorption reaction of the native GeO_2. The higher Ge^{4+} content (46%) in the XPS with two Al_2O_3 passivation cycles compared with the no passivation case (40%) revealed that the ALD process using TMA and O_3 preferred oxidation of the Ge surface to GeO_2 compared with the progression of the desorption reaction, which is a reasonable consequence of the exposure of the cleaned Ge surface (by TMA) to O_3. The increased Al_2O_3 ALD cycles decreased the Ge^{4+} content, which could be understood because the oxidation of Ge to GeO_2 was retarded by the increased Al_2O_3 thickness, while the desorption reaction started to increase.

When the 2-nm-thick SiO_2 capping layer was adopted on the 5-nm-thick La-silicate/(two cycles) Al_2O_3 passivated films, the

dx.doi.org/10.1021/am5012172 | ACS Appl. Mater. Interfaces 2014, 6, 7885–7894

Ge concentration in the film increased (Figure 11). According to the data shown in Figure 6b and the related discussions above, the 5-nm-thick La-silicate/(2 cycles) Al_2O_3passivated films had a negligible Ge concentration and the increased Ge concentration was induced by the additional SiO_2 capping process. When compared with the ALD processing time of 6-nm-thick La-silicate film in Figure 6, the 5-nm-thick La-silicate film required a 416 s shorter processing time, and the additional 2-nm-thick SiO_2 film required an ALD processing time of 375 s. Therefore, the increased Ge concentration in the film was not caused by the overall increase in the ALD processing time. As described previously, the two-cycle Al_2O_3 passivation process may have already removed the native GeO_2. The only possible source of GeO (the Ge contents in the La-silicate film) must have originated from the reaction between the oxidized GeO_2 (by the O_3 in ALD process) and the Ge substrate. As this was far less active than the desorption reaction between the native GeO_2 and Ge, the amount of GeO produced was quite small. This small amount might have volatilized through the La silicate, even though it possessed certain barrier properties over the GeO diffusion, so that the La-silicate/Al_2O_3 passivation films did not contain a considerable amount of Ge impurities. As can be understood from Figure 1e, SiO_2 appeared to have the highest barrier properties against diffusion of the GeO. Therefore, the small amount of GeO formed could not diffuse through the La-silicate layer when it was coated with SiO_2. This must have suppressed the desorption reaction at the interface and the achieved electrical performance was optimum. This is in agreement with the study by Oh and Campbell, where they reported that the SiO_2 capping layer blocked the absorption of oxygen and prevented further oxidation of the Ge.[29] From these results, it is concluded that the deterioration of the C−V characteristics in the GeO_2/Ge MOS capacitors originated from the interface reaction, driving volatilization of the GeO.

V. CONCLUSIONS

Three approaches were taken in this work to improve the electrical performances of high-k La-based oxide films on Ge-substrates. They were increasing the Si concentration in the La_2O_3 films, adopting an ultrathin Al_2O_3 passivation layer at the La-silicate/Ge interface, and capping the La-silicate/ultrathin Al_2O_3 gate stack layer with a 2-nm-thick SiO_2 layer. The electrical properties of the MOSCAPs were studied by the amount of hysteresis in their C−V curves, and the degradation in the V_{FB} and D_{it} using CVS tests. In general, increasing the Si concentration in the La-silicate films (up to 35%) was an effective method in improving the electrical performance. This was because suppression of the desorption reaction between the native GeO_2 and Ge substrate was induced by the lower diffusion of Ge (or GeO) through the La-silicate film, compared with pure La_2O_3. However, a Si concentration that was too high decreased the k value. Therefore, the Si concentration was fixed at 25%, and the interface with the Ge substrate was passivated with an ultrathin ALD Al_2O_3 layer. The ALD process using TMA and O_3 induced two aspects in terms of the desorption reaction; TMA reduced the native GeO_2, which suppressed the subsequent desorption reaction. In contrast, the prolonged ALD process induced adverse oxidation of Ge to GeO_2, which eventually induced the desorption reaction. Therefore, two ALD cycles of Al_2O_3 resulted in the optimal condition among the different cycle numbers that were attempted. The hysteresis in the C−V curves could be decreased to ∼240 mV under this condition, while the La-silicate films with no Al_2O_3 passivation showed a hysteresis voltage of ∼900 mV. The C−V hysteresis was further decreased to ∼100 mV (best case 50 mV) by adopting a SiO_2 capping layer. This was believed to be caused by further suppression of the deleterious desorption reaction by almost completely suppressing the outward diffusion of GeO, which could have formed by the minute reaction between the O_3-induced GeO_2 and Ge.

This work could provide a viable guideline in suppressing the C−V hysteresis by focusing on the possible routes to induce an adverse desorption reaction on Ge substrates for future MOSFETs. Although MOSFET fabrication includes various thermal treatments, which are not dealt with in this work, this work could also provide researchers with a viable reference to alleviate the adverse reaction that could be induced during the thermal treatment of the gate stack.

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Notes

The authors declare no competing financial interest.

ACKNOWLEDGMENTS

This work was supported by the Converging Research Center Program (2013K000158) through the Ministry of Science, ICT, and Future Planning, Republic of Korea, and also supported by Samsung Electronics. Co., Ltd. [Process development of Ge and III−V compound semiconductor for high mobility channel devices] and Samsung Display. Co., Ltd. [Fracture Analysis of an encapsulation layer for flexible OLED using electrical methods].

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